a plurality of conductive posts electrically connected to the semiconductor device, said conductive posts having outer edges; [and]

a resin covering over said device main surface for sealing said device main surface, said resin covering leaving exposed said device peripheral side surface; and

means for mounting the device onto a circuit board by soldering, including a plurality of conductive bumps respectively positioned on an outer end of each of the conductive posts for soldering onto the circuit board, wherein [a peripheral edge of a resin covering for sealing a surface of the semiconductor device and an] the outer [edge] edges of [the] said conductive [post] posts are separated from said device peripheral edges by a distance narrower than a height of the conductive post.

2. (Previously Amended) A semiconductor apparatus according to claim 1, wherein the distance is in a range between 50 and 100 micrometers.

3. (Previously Amended) A semiconductor apparatus according to claim 1, wherein the semiconductor device is provided with a plurality of electrode pads connected to the conductive posts, the electrode pads being arranged on a line extending in a center portion of the semiconductor device.

4. (Original) A semiconductor apparatus according to claim 1, wherein the semiconductor device is provided with a plurality of electrode pads connected to the conductive posts, each of the electrode pads being arranged between two adjacent conductive posts.

5. (Original) A semiconductor apparatus according to claim 1, wherein the semiconductor device is provided with a plurality of electrode pads connected to the conductive posts, each of the electrode pads being arranged directly under a corresponding conductive post.

6. (Original) A semiconductor apparatus according to claim 1, wherein the conductive bumps are of solder.

7. (Currently amended) A semiconductor apparatus comprising:

a semiconductor device having a device main surface, peripheral device edges bounding the main surface and a peripheral side surface extending from said peripheral device edges and bounding said device;

a plurality of conductive posts electrically connected to the semiconductor device, said posts having post outer ends and post peripheral surfaces extending from said device main surface to said post outer ends, said post peripheral surfaces having post inner end portions extending from said device main surface, and post outer end portions extending from said post inner end portions to said post outer ends;

means for mounting the device onto a circuit board by soldering, including a plurality of conductive bumps respectively positioned on said post outer ends for soldering onto the circuit board; and

a molding resin covering said device main surface, wherein said molding resin includes a step along the entirety of a peripheral portion of said device main [portion]

surface, the step covering said post inner end portions, while leaving exposed said post outer end portions and said device peripheral side surface.

8. (Original) A semiconductor apparatus according to claim 7, wherein the difference in level between the upper portion and lower portion of the step is half of a thickness of the mold resin.

9. (Previously Amended) A semiconductor apparatus according to claim 7, wherein the difference in level between the upper portion and lower portion of the step is in a range between 40 and 60 micrometers.

10. (Original) A semiconductor apparatus according to claim 7, wherein the conductive bumps are of solder.

11. (Currently Amended) A semiconductor apparatus comprising:

a semiconductor device, said device having a device main surface, peripheral device edges bounding the main surface and a peripheral surface extending from said peripheral device edges and bounding said device;

a plurality of conductive posts electrically connected to the semiconductor device;

means for mounting the device onto a circuit board by soldering, including a plurality of first conductive bumps respectively positioned on an outer end of each of the conductive posts for soldering onto the circuit board;

a molding resin covering [a] said main surface of the semiconductor device without covering a peripheral side surface of the conductive posts; and

an insulating layer formed on [a] said peripheral surface of the semiconductor device between [an upper] said main surface of the semiconductor device and the conductive posts, wherein the molding resin is shaped to have a peripheral side surface on the identical plane with the peripheral side surface of the semiconductor device.

12. (Original) A semiconductor apparatus according to claim 11, wherein the insulating layer is formed to have a width of 100 to 200μm.

13. (Previously Amended) A semiconductor apparatus according to claim 11, further comprising a plurality of second conductive bumps each provided on a respective peripheral side surface of a respective one of the conductive posts.

14. (Previously Amended) A semiconductor apparatus according to claim 11, wherein the first conductive bumps are of solder.

15. (Previously Amended) A method for fabricating a semiconductor apparatus according to claim 7, comprising the steps of:

providing a semiconductor wafer on which a plurality of semiconductor devices are formed, each of the semiconductor device having electrode pads thereon;

providing a plurality of conductive post connected to the electrode pads of the semiconductor devices;

molding the semiconductor devices with a molding resin so that an upper surface of the molding resin is on the same plane with upper surfaces of the conductive posts;

removing a part of the molding resin to be located at a peripheral edge so that the peripheral edge of the molding resin has a step, the step having upper and lower level portions;

providing conductive bumps on outer ends of the conductive posts; and

dicing the semiconductor wafer to form a plurality of individual semiconductor apparatuses.

16. (Original) A method according to claim 15, wherein the difference in level between the upper portion and lower portion of the step is half of a thickness of the mold resin.

17. (Previously Amended) A method according to claim 15, wherein the difference in level between the upper portion and lower portion of the step is in a range between 40 and 60 micrometers.

18. (Original) A method according to claim 15, wherein the conductive bumps are of solder.

19. (Previously Amended) A method for fabricating a semiconductor apparatus according to claim 11, comprising the steps of:

providing a semiconductor wafer on which a plurality of semiconductor devices are formed, each of the semiconductor devices having electrode pads thereon;

forming grooves in the semiconductor wafer at portions corresponding to dicing lines of the semiconductor wafer;

forming an insulating layer on the wafer so that the grooves are filled with the insulating layer but a part of each electrode pad of the semiconductor devices is not covered with the insulating layer;

forming a metal layer on the insulating layer and the part of each electrode pad, not covered with the insulating layer;

forming a rewiring layer on the metal layer;

providing a conductive post material extending across each of the grooves;

molding the semiconductor wafer with a molding resin so that an upper surface of the molding resin is on the same plane with upper surfaces of the conductive post material across each of the grooves;

providing a conductive bump material on the conductive post material; and

dicing the semiconductor wafer at the grooves to form a plurality of individual semiconductor apparatuses.

20. (Original) A method according to claim 19, further comprising the steps of:

expanding the distance between two adjacent semiconductor devices after the dicing process; and

reflowing the distanced semiconductor devices so as to form a conductive soldering bump on a peripheral side surface of each of the conductive posts.

21. (Original) A method according to claim 19, wherein the insulating layer is formed to have a width of 100 to 200μm.

22. (Original) A method according to claim 19, wherein the conductive bumps are of solder.

23. (Previously Added) A semiconductor apparatus according to claim 11, wherein the peripheral side surface of each conductive post is formed in the same plane as that of the peripheral side surface of the semiconductor device.